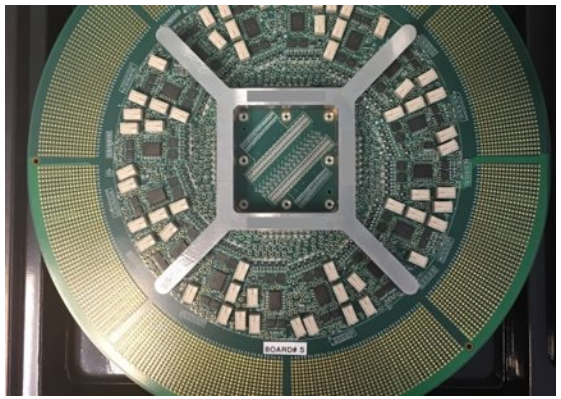

# P² Interposer Space Translation

# Current Pitch Translation Challenges (Before)

Test Interface design engineers are tasked with developing solutions requiring very tight pitches, with future roadmaps pushing even tighter. Pitches at 150 µm and tighter are becoming common. While the industry has current solutions for these challenges, they are not ideal from a cost, reliability and schedule perspective.

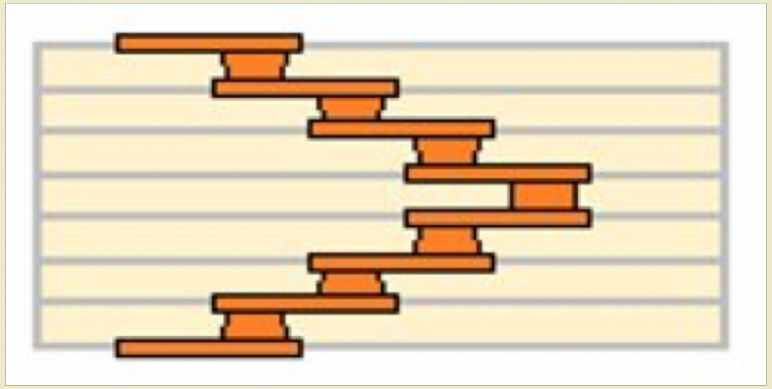
**Current Solutions**:

- Increased PCB layer count (cost & reliability concerns)
- PCB potentially un-manufacturable (or limited on FABS)
- Longer design schedules, impacting production release
- MLO/MLC solutions with increased cost, risk & schedule
- Increased use of blind/buried vias or micro/laser vias
- Limited site count, due to interface density



*High Density Probe Card*
*(Site Count Limited)*

MLO/MLC Design Internal View

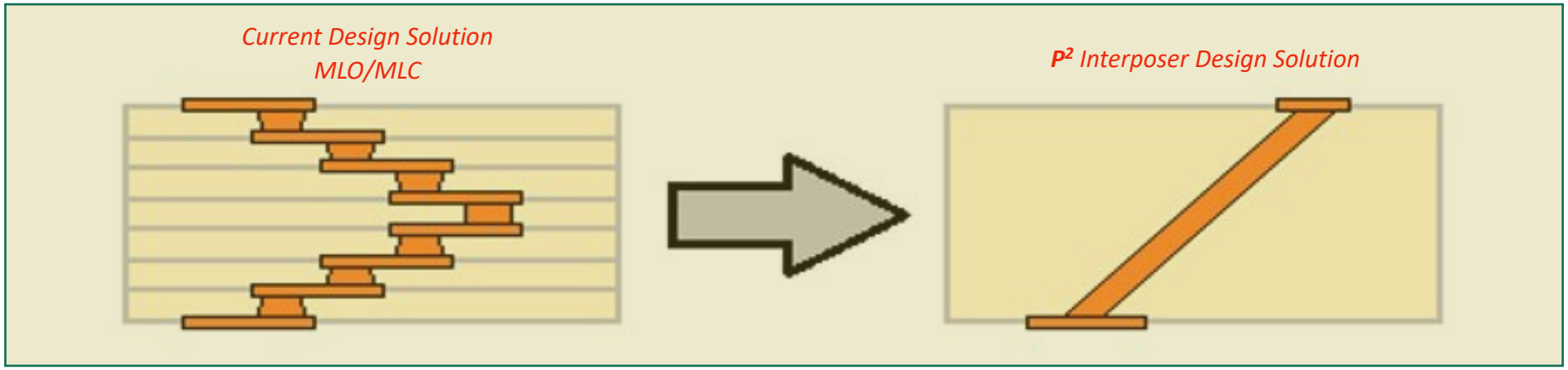


**Solution Weaknesses**:

- Blind & buried vias
- High layer count
- Increased design impact to overall schedule
- Increased cost and risk to overall project
- DFM reliability concerns, low yield
- Requires permanent attachment to PCB

# Introducing the P² Interposer (The Bridge)

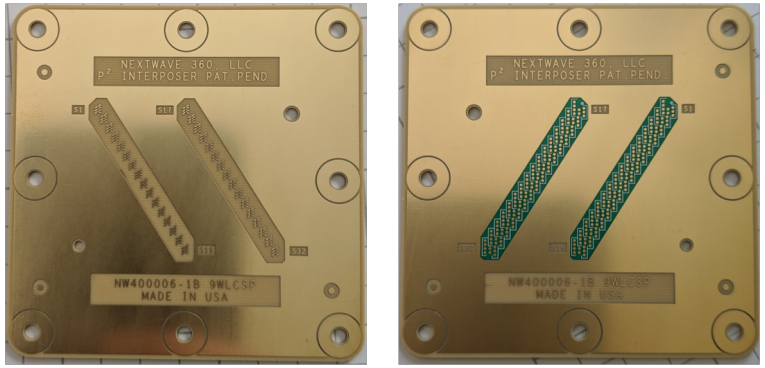
NextWave 360 Engineers are very experienced working through the current pitch translation challenges and have developed innovative solutions that will change the way test interface hardware is designed and manufactured in the future. To tackle the challenges with tight pitch designs, NextWave 360 has developed the **P²** Space Translation Interposer.




The P² Interposer

**P² Design Features over the Current Solutions**:

- Straight through angled vias (there are no blind or buried vias)
- 2-layer monolithic substrate (can be customized for your solutions)
- Vias filled with conductive or non-conductive epoxy, per your requirements
- Pads, typical PCB plate up including nickel/gold



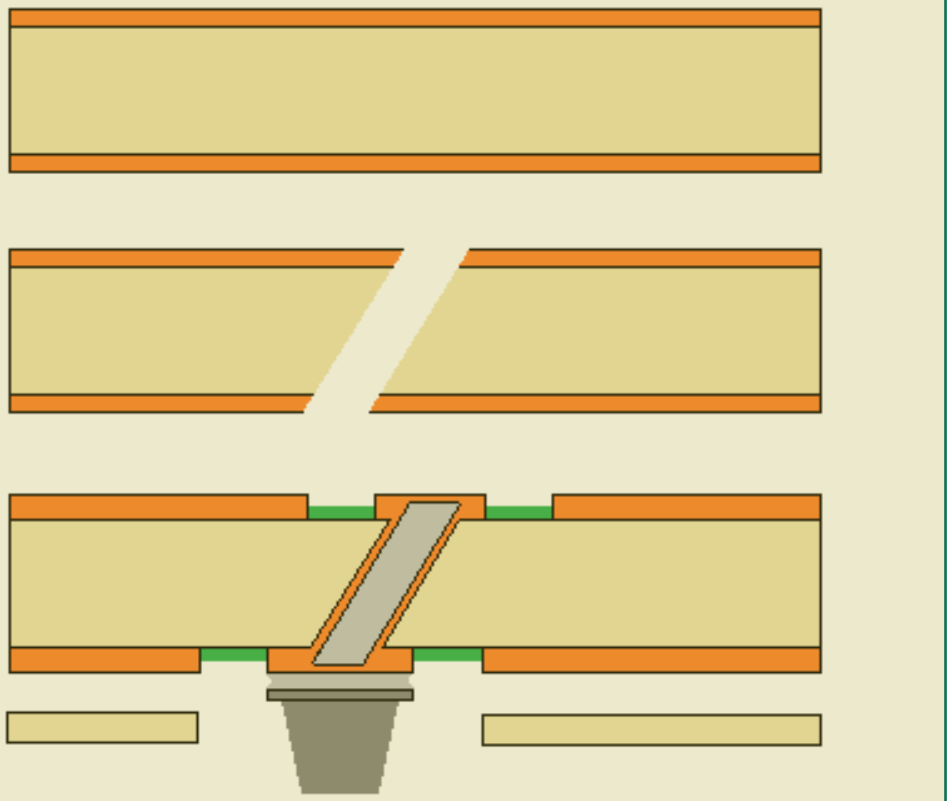

*Patent Pending # 62774910*

# Fabrication and Assembly Process

**Fabrication & Assembly Highlights**:

- Substrate construction
- CNC processes
- Standard PCB finishing steps
- Standard reflow attachment or elastomer pin Assembly
- Compression stop

*$P^2$ Fabrication Build Up With Elastomer Pin*



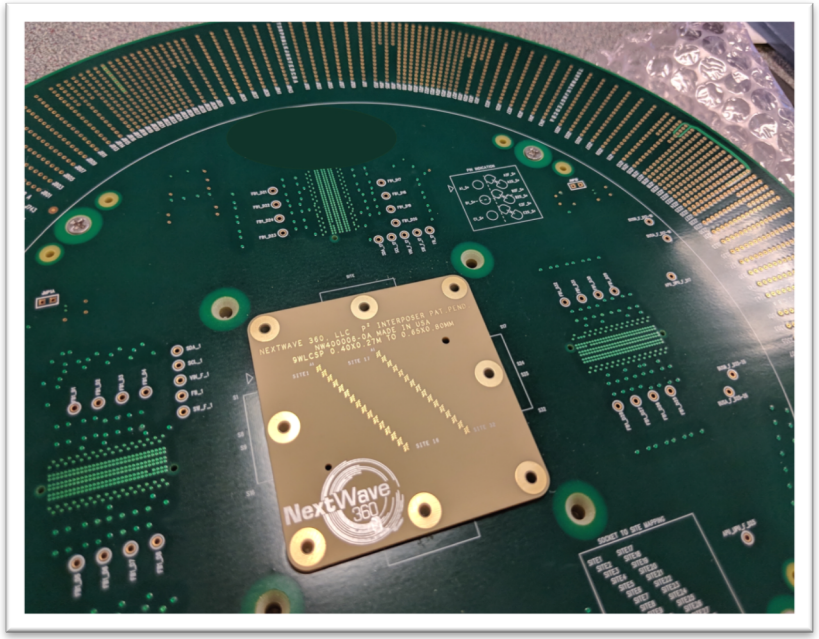
# P² Pitch Translation (After)

The NextWave 360 P² Interposer innovation is making an impact in the semiconductor interface application world. The P²'s advantage is in its simplicity in design. Imagine moving forward with your complex interface solutions, using the P² technology and the benefits it provides:

**Why use the P² Interposer?**:

- **Design Simplification** - Designs can be complete in as little as one day, providing a significant reduction in the overall design schedule.
- **Simplified Fabrication** – The P² interposer can be manufactured and delivered
  far before the FAB of the mother PCB is complete.
- **Reduced Risk** - The P² interposer reduces DFM complexity, allowing for lower layer counts and higher FAB output yield.
- **Cost Competitive** – Reduces cost of the P² solution vs. an MLO/MLC and reduces the cost of the PCB, due to complexity reduction.
- **Multiple Attachment Methods** – Standard reflow, Elastomer pin assembly or Sintering – Dependent on customer preferences

*Implementation of the P² Interposer reducing PCB complexity and enabling a higher site count solution*



# $P^2$ Attachment Methodologies

To meet our customer's needs and preferences, we've designed the $P^2$ Interposer with the capability of multiple methods of attaching the interposer to the PCB.

**Elastomer Pins**:

- Simple installation on-site at the same time as the probe head or socket
- Simple removal on-site
- Not a permanent addition to the PCB, for ease of repair or replacement
- Can move around for engineering work and correlation

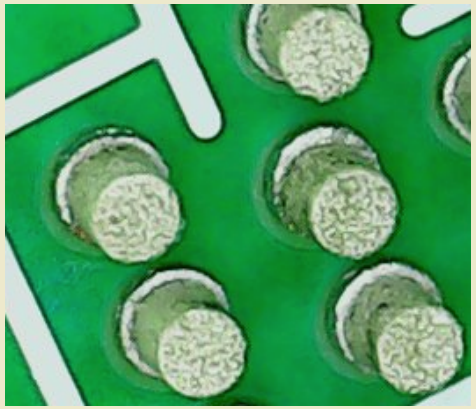
**Solder Reflow**:

- The interposer can be attached via reflow at the same time as the PCB components are attached, minimizing schedule impact
- Provides a solid connection and is X-Ray verified
- Can be removed if needed

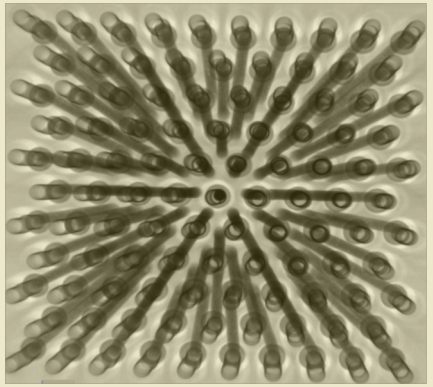
**Sintering**:

- Provides a permanent connection to the PCB
- Thin substrates where planarity is key
- Eliminates the possibility of "potato-chipping"

*Elastomer pins applied to the $P^2$ Interposer*

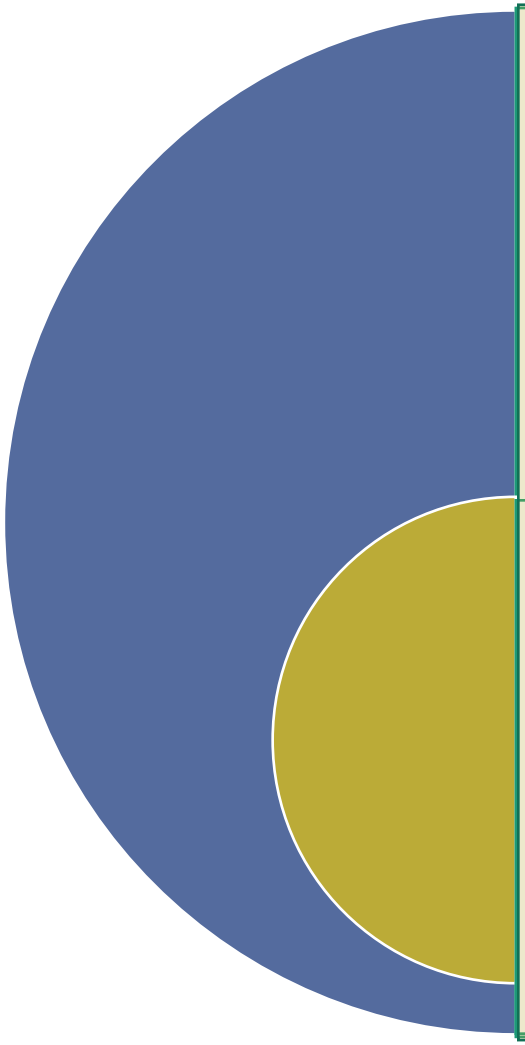


*X-Ray Images of a reflow connection*



# P² Interposer Key Attributes

## P² Interposer Attributes



Pitch gain capability up to 400%

Pitch capability as low as 0.15mm

1 Mil/Linear Inch planarity

Socket/probehead alignment within 10 microns

Up to 25GHz of high quality performance

Characterized up to 10A continuous

**Design in as little as one day**

**Delivery in about 3 weeks**

Removes barriers to DFM challenges, increasing FAB yield

Allows for more FAB houses to compete for the business

Increases signal integrity, lowers layer count

Reduces overall cost

Completely tester agnostic

Please feel free to contact me directly with any questions or to organize a meeting to further discuss how NextWave 360's applications and interface hardware engineering team can help your test floor run more efficiently.

"We differentiate ourselves with our approach to customer satisfaction, project management, regular communication, check-steps and our focus on design for manufacturability. Our relationships with several FAB houses ensures that we can deliver your project on time and on budget with the highest level of quality expected"

Best Regards,

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# NextWave 360 – About Us

**NextWave 360** is a full-service semiconductor test solutions engineering group with a mission to support our customer's most critical and time sensitive product & project goals. Through collaboration and partnerships, we work together to enable the continued innovation of technical solutions bridging the technology gap between our customers test interface challenges

Our Team Customers Quality Delivery

*From start to finish, our **Team** is fully engaged with our **Customers** to ensure every requirement has been met to the highest **Quality** standard from the initial concept to the **Delivery** of the final product.*